REMARKS

This Response responds to the Office Action dated July 14, 2006 in which the Examiner rejected claims 1, 3-4 and 6 under 35 U.S.C. §102(b) and rejected claims 7-9 under 35 U.S.C. §103.

Claim 3 claims a semiconductor integrated circuit comprising a plurality of modules having their operations controlled by respective chip select signals. Each module has a plurality of memory cells and each module has a control circuit controlling an operation of reading or writing data from or into the memory cell. The plurality of modules receive a common address signal sent through a common internal address bus, where the plurality of modules have word lines different in number. The control circuit included in a module that does not have a maximum number of word lines controls an operation of reading or writing data from or to the memory cell in a test mode, irrespective of a value of the chip select signal, only when values of one or more prescribed bits forming an address signal are prescribed values.

Through the structure in the claimed invention having a) a plurality of modules having different number of word lines and b) in a module that does not have a maximum number of word lines, a control circuit, irrespective of a chip select signal, controls an operation of reading or writing data in a test mode only when values of prescribed bits of an address signal are prescribed values, as claimed in claim 3, the claimed invention provides a semiconductor integrated circuit which prevents the same word line from being activated at different times in a memory test mode. The prior art does not show, teach or suggest the invention as claimed in claim 3.

Claims 1, 3-4 and 6 were rejected under 35 U.S.C. §102(b) as being anticipated by *Kawamata* (U.S. Publication No. 2001/0042231).

Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. §102(b). The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, Applicants respectfully request the Examiner withdraws the rejection to the claims and allows the claims to issue.

Kawamata appears to disclose in Figure 5 a plurality of fail information memories 110-113 for a main memory array and one fail information memory 20 for redundant cells, each having addresses A0-A21. Thus nothing in *Kawamata* shows, teaches or suggests a plurality of modules having a different number of word lines, as claimed in claim 3. Rather, *Kawamata* teaches away from the claimed invention since all of the main cell arrays and redundant cells contain the same number of address lines.

Additionally, *Kawamata* discloses both channel data and a redundancy signal input to the main memories and redundant memory. Nothing in *Kawamata* shows, teaches or suggests that each module has a control circuit controlling the operation of reading or writing to or from the memory cells of the module as claimed in claim 3. Rather, *Kawamata* only discloses channel data bits and a redundancy signal and thus does not disclose a control circuit at every module.

Also, *Kawamata* merely discloses at paragraph [0057] supplying the fail signal of the channel data bit D0 to a chip select terminal (CSB) in order to indicate whether information should be written into the module. Thus nothing in *Kawamata* shows, teaches or suggests controlling reading or writing irrespective of a value of a chip

select signal in a test mode as claimed in claim 3. Rather, the chip select terminal in *Kawamata* is activated when information is to be written into the cell.

Finally, *Kawamata* merely discloses a redundancy signal which indicates testing of the main cell array or redundant cells, and if the redundant cells are to be tested, the write enable terminal is inactivated so that the fail information memory is inactivated and the memories are put in a condition unable to write ([0059] – [0061]). Thus, nothing in *Kawamata* shows, teaches or suggests controlling reading or writing based upon values of bits in an address signal which are at prescribed values as claimed in claim 3. Rather, *Kawamata* only discloses controlling reading/writing based upon the redundancy signal.

Since nothing in *Kawamata* shows, teaches or suggests a) modules having different number of word lines, b) each module having a control circuit controlling the operation of reading or writing, c) controlling the operation of reading or writing irrespective of a chip select value in a test mode and c) controlling reading or writing in test mode only when values of prescribed bits in an address signal are prescribed values as claimed in claim 3, applicants respectfully request the Examiner withdraws the rejection to claim 3 under 35 U.S.C. §102(b).

Claims 1, 4 and 6 depend from claim 3 and recite additional features. Applicants respectfully submit that claims 1, 4 and 6 would not have been anticipated by *Kawamata* within the meaning of 35 U.S.C. §102(b) at least for the reasons as set forth above. Therefore, applicants respectfully request the Examiner withdraws the rejection to claims 1, 4 and 6 under 35 U.S.C. §102(b).

Claims 7-9 were rejected under 35 U.S.C. §103 as being unpatentable over *Kawamata* and further in view of *Urakawa*.

Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. §103. The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, Applicants respectfully request the Examiner withdraws the rejection to the claims and allows the claims to issue.

As discussed above, since nothing in *Kawamata* shows, teaches or suggests the primary features as claimed in claim 3, Applicants respectfully submit that the combination of the primary reference with the secondary reference to *Urakawa* would not overcome the deficiencies of the primary reference. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claims 7-9 under 35 U.S.C. §103.

Thus, it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested. Should the Examiner find that the application is not now in condition for allowance, applicants respectfully request the Examiner enters this Amendment for purposes of appeal.

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is requested to contact, by telephone, the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

BUCHANAN INGERSOLL & ROONEY PC

Date: December 12, 2006 By: _____

Ellen Marcie Emas
Registration No. 32131

P.O. Box 1404
Alexandria, VA 22313-1404
703 836 6620